IN THE CLAIMS:

Please cancel claims 19 and 23 without prejudice or disclaimer.

Please amend the claims as follows:

3. (Twice Amended) A semiconductor device, comprising:

a first transistor having a first gate put between a first source and a first drain;

a second transistor arranged adjacent to said first transistor, said second transistor having a second gate put between a second source and a second drain;

a first dummy gate arranged between said first drain and said second source;

a second dummy gate arranged adjacent to said first source; and

a third dummy gate arranged adjacent to said second drain,

wherein said first and second gates, and said first, second and third dummy gates are substantially evenly spaced, and

wherein said first dummy gate is arranged parallel to said first gate.

5. (Twice Amended) A semiconductor device comprising:

a first transistor having

a first source,

a first drain,

a first gate arranged between said first source and said first drain,

a first contact hole formed on said first source and arranged at a first distance from said first gate, and

a second contact hole formed on said first drain and arranged at a second distance from said first gate, said second distance being the same as said first distance;

a second transistor having

a second source,

a second drain,

a second gate arranged between said second source and second drain,

a third contact hole formed on said second source and arranged at a third distance from said second gate, and

a fourth contact hole formed on said second drain and arranged at a fourth distance from said second gate, said fourth distance being the same as said third distance;

a first dummy gate set between said first drain and said second source;

a second dummy gate set next to said first source; and

a third dummy gate set next to said second drain,

wherein said first gate, said second gate, said third gate, said first dummy gate, said second dummy gate, and said third dummy gate are substantially evenly spaced, and

wherein said first dummy gate is set parallel to said first gate.

B3 6. (Twice Amended) A semiconductor device including first and second transistors each having a terminal commonly connected to a node, said device comprising:

a first gate electrode layer of said first transistor;

a first electrode layer of said first transistor coupled to a first contact hole;

a second electrode layer of said first transistor coupled to a second contact hole;

a second gate electrode layer of said second transistor, said second gate electrode layer being electrically separated from said first gate electrode layer;

a third electrode layer of said second transistor coupled to a third contact hole;

a fourth electrode layer of said second transistor coupled to a fourth contact hole, said fourth electrode layer electrically coupled to said second electrode layer as said terminal,

wherein said first gate electrode layer, said first electrode layer, said second electrode layer, said second gate electrode layer, said third electrode layer, and said fourth electrode layer are arranged so that a first distance between said first contact hole and said first gate electrode layer is substantially the same as a second distance between said third contact hole and said second gate electrode, and a third distance between said second contact hole and said first gate electrode layer is substantially the same as a fourth distance between said fourth contact hole and said second gate electrode layer while a mask for forming said first to fourth contact holes is misaligned, and

B3

wherein said first electrode layer is a source of said first transistor, said second electrode layer is a drain of said first transistor.

B4

8. (Amended) The device as claimed in claim 7, wherein said third electrode layer is a source of said second transistor, and said fourth electrode layer is a drain of said second transistor.

11. (Twice Amended) A semiconductor device, comprising:

a first source diffusion region;

a first drain diffusion region;

a second source diffusion region;

a second drain diffusion region,

said first source diffusion region, said first drain diffusion region, said second source diffusion region, and said second drain diffusion region being arranged in that order on a line extending in a first direction, said first and second source diffusion regions and said first and second drain diffusion regions being surrounded by an element isolation region;

B5

a first gate electrode formed between said first source and drain diffusion regions and extending in a second direction;

a second gate electrode formed between said second source and drain diffusion regions and extending in said second direction;

a first source electrode formed over said first source diffusion region and connected with said first source diffusion region through a first contact hole;

a first drain electrode formed over said first drain diffusion region and connected with said first drain diffusion region through a second contact hole;

a second source electrode formed over said second source diffusion region and connected with said second source diffusion region through a third contact hole;

a second drain electrode formed over said second drain diffusion region and connected with said second drain diffusion region through a fourth contact hole;

a first dummy gate electrode arranged between said first drain and said second source electrodes on said element isolation region;

a second dummy gate electrode arranged on said element isolation region so that said

first source electrode is sandwiched between said second dummy gate electrode and said first gate electrode; and

a third dummy gate electrode arranged on said element isolation region so that said second drain electrode is sandwiched between said third dummy gate electrode and said second gate electrode,

wherein a first distance between said first dummy gate electrode and said first gate electrode and a second distance between said first dummy gate electrode and said second gate electrode are substantially the same as each other.

12. (Amended) The device as claimed in claim 11, wherein a first transistor includes said first source diffusion region, said first drain diffusion region, and said first gate electrode as one of N channel transistor pair and a second transistor includes said second source diffusion region, said second drain diffusion region, and said second gate electrode as the other of said N channel transistor pair electrically to connect said first drain electrode with said second drain electrode.